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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,464	03/05/2004	Liang-Yun WANG	MTKP0143USA	2463

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EXAMINER	
PHAN, DEAN	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
11/19/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/708,464	WANG, LIANG-YUN	
	Examiner	Art Unit	
	Dean Phan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/27/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 09/19/2007 have been fully considered. The newly added limitation in combination with the existing elements of claim(s) alters the scope of the claims. Therefore, the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 9-16, 19-25, 28-35, & 38-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (US 20030084221, hereafter Jones), in view of ATA Packet Interface for CD-ROM (Revision 2.6 proposed, hereafter Pub).

As per Claims 1, Jones discloses, "An electronic system comprising:

a host; (pc 20 in Fig. 9)

a controller electrically coupled to the host (chip 40 in Fig. 9) through a single port (46 in Fig. 9) of a predetermined interconnection means (IDE interface ¶[00460, the

predetermined interconnection means being designed for providing the host access to a maximum of N devices (IDE devices connected to the host by interface ¶[0046]); and

M peripheral devices electrically coupled to the controller; (devices 62, 64, 66, 68, and 70 in Fig. 9) wherein M is greater than N (host can choose which of the connected devices to access by chip 40 in Fig. 9) and

the controller allows the host to access the peripheral devices using the single port. (chip 40 connects pc 20 through connector 46 all Fig. 9).

Jones does not disclose the host (Fig. 9 CPU 92) modifies predetermined existing fields in packets/commands (*Instead, discloses new commands to identify a target device*). However, ATAPI packet command is a derivative of the standard IDE interface. ATAPI is a special protocol that was developed to allow devices like CD-ROM drives and tape drives to attach to regular IDE controllers normally used for hard disks. According to the specification, An ATAPI packet command contains many predetermined existing fields such as an operation code, LBA, MSB... Each operation code is sent from a host computer to an IDE device as a command to specify the operation to be performed. Pub discloses reserved operation codes in ATAPI that are used for future standardized commands. The use and interpretation of those operation codes may be specified by future extensions to this or other standards (page 15, 87, 92). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement ATAPI packets with new commands of Jones, by using the host computer to modify the predetermined existing fields with new commands to specify the target peripheral device, in order to standardize and extend the ability of

specifying a target peripheral device of Jones' invention in ATA packet interface environment (*see* pages 15, 87, 92).

As per Claims 9, 11, 20, 28, 30, 39, & 47, Jones further discloses, "The electronic system of claim 1, wherein the M peripheral devices include a first peripheral device (flash-memory cards 62-68 in Fig. 9) and a second peripheral device (disk 70 in Fig. 9), and the controller (chip 40 in Fig. 9) directly transfers data stored on the first peripheral device to the second peripheral device without buffering the data in the host." Copying from flash-memory cards to removable disk without being connected (or buffering data) in the host (pc) (¶[0092 & 0093]). As per the limitations of memory for the extra devices (in Claim 39), Jones discloses, "...and a memory (RAM 94 in Fig. 10) for storing the data, wherein the memory is shared by the extra (M-N) devices." (*RAM 94 is shared by chip 40 (Fig. 9) by the devices connected to the controller and used to store (buffer) data* ¶[0100])

As per Claims 2, 12, 21, 31, & 40, Jones discloses, "The electronic system of claim 1, wherein the predetermined interconnection means is an Integrated Drive Electronics (IDE) bus (IDE interface ¶[0046]) or a Serial AT Attachment (SATA) interface. Claims 12, 21, 31, & 40 are rejected in similar fashion.

As per Claims 3, 13, 22, 32, & 41, Jones discloses, "The electronic system of claim 1, wherein the existing task file is an IDE task file (Pub, page 17)". Claims 13, 22, 32, & 41 are rejected in similar fashion.

As per Claims 4, 14, 23, 33, & 42, Jones discloses, "The electronic system of claim 3, wherein the predetermined fields are control codes (Pub, page 87; Jones

¶[0101]) to specify the target peripheral device." Claims 14, 23, 33, & 42, are rejected in similar fashion.

As per Claims 5, 15, 24, 34, & 43, Jones discloses, "The electronic system of claim 1, wherein the M peripheral devices electrically coupled to the controller at least comprise an optical storage device (cd-rom ¶[0119]) and a non-volatile storage device. (62-68 in fig. 9)" Claims 15, 24, 34, & 43, are rejected in similar fashion.

As per Claims 6, 16, 25, 35 & 44, Jones discloses, "The electronic system of claim 5, wherein the non-volatile storage device is a flash card access device (62-68 in fig. 9) or a hard-disk drive." Claims 16, 25, 35, & 44 are rejected in similar fashion.

Claims 7, 8, 17, 18, 26, 27, 36, 37, & 45, 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (US 20030084221) in view of ATA Packet Interface for CD-ROM (Revision 2.6 proposed), in further view of Fuller (US Pat# 4809164).

As per Claims 7, 8, 17, 18, 26, 27, 36, 37, & 45, 46, Jones and Pub discloses, the electronic system of claim 1, but do not teach the host schedules packets sent to the M peripheral devices according to a priority ranking wherein the priority ranking is a dynamic ranking that varies according to operations or speed settings of the peripheral devices. However, in the same field of art, Fuller teaches an electronic system, which comprise a processor and plural peripheral devices. Fuller teaches an improvement of the prioritization technique wherein a higher priority is given to those devices that must unload data quickly and a lower priority is given to slower devices (col 2 lns 35-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of

invention to implement the teachings of Fuller into Jones' system, by scheduling packets sent to the M peripheral devices according to according to operations or speed settings of the peripheral devices, in order to provide an improved order of communication between the host and peripheral devices. (col 1 lns 5-40, col 2 lns 35-51). Claims 17, 18, 26, 27, 36, 37, & 45, 46 are rejected in similar fashion.

Examiner's note:

Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dean Phan whose telephone number is (571) 270-1002. The examiner can normally be reached on Mon - Thu; 9:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on (571) 272 4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

dp

HENRY TSAI
SUPERVISORY PATENT EXAMINER

11/10/07